PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference TW/ZWL/cat/E.2005000684	FOR FURTHER ACTION	See Form PCT/IPEA/416
International application No. PCT/SG2005/000022	International filing date *(day/month/year)* 27 January 2005	Priority date *(day/month/year)* 19 February 2004

International Patent Classification (IPC) or national classification and IPC

Int. Cl.

G11C 11/34 (2006.01)

Applicant

AGENCY FOR SCIENCE, TECHNOLOGY AND RESEARCH et al

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 3 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. [X] *(sent to the applicant and to the International Bureau)* a total of **8** sheets, as follows:
      - [X] sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      - [ ] sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.

   b. [ ] *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or table related thereto, in electronic form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).
4. This report contains indications relating to the following items:

[X]	Box No. I	Basis of the report
[ ]	Box No. II	Priority
[ ]	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
[ ]	Box No. IV	Lack of unity of invention
[X]	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
[ ]	Box No. VI	Certain documents cited
[ ]	Box No. VII	Certain defects in the international application
[ ]	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
19 December 2005	30 January 2006
Name and mailing address of the IPEA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	Authorized Officer **Matthew Hollingworth** Telephone No. (02) 6283 2024

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/SG2005/000022

Box No. I Basis of the report

1. With regard to the **language,** this report is based on:

[X] The international application in the language in which it was filed

[ ] A translation of the international application into , which is the language of a translation furnished for the purposes of:

[ ] international search (under Rules 12.3(a) and 23.1 (b))

[ ] publication of the international application (under Rule 12.4(a))

[ ] international preliminary examination (Rules 55.2(a) and/or 55.3(a))

2. With regard to the **elements** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

[ ] the international application as originally filed/furnished

[X] the description:

pages **1-14** as originally filed/furnished
pages* received by this Authority on with the letter of
pages* received by this Authority on with the letter of

[X] the claims:

pages as originally filed/furnished
pages* as amended (together with any statement) under Article 19
pages* **15-22** received by this Authority on **16 December 2005** with the letter of **the same date**
pages* received by this Authority on with the letter of

[X] the drawings:

pages **1-6** as originally filed/furnished
pages* received by this Authority on with the letter of
pages* received by this Authority on with the letter of

[ ] a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing.

3. [X] The amendments have resulted in the cancellation of:

[ ] the description, pages
[X] the claims, Nos. **12, 13, 18, 23, 24**
[ ] the drawings, sheets/figs
[ ] the sequence listing *(specify)*:
[ ] any table(s) related to the sequence listing *(specify)*:

4. [ ] This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

[ ] the description, pages
[ ] the claims, Nos.
[ ] the drawings, sheets/figs
[ ] the sequence listing *(specify)*:
[ ] any table(s) related to the sequence listing *(specify)*:

* *If item 4 applies, some or all of those sheets may be marked "superseded."*

Box No. V **Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	**1-11, 14-17, 19-22, 25-34**	**YES**
	Claims		**NO**
Inventive step (IS)	Claims	**1-11, 14-17, 19-22, 25-34**	**YES**
	Claims		**NO**
Industrial applicability (IA)	Claims	**1-11, 14-17, 19-22, 25-34**	**YES**
	Claims		**NO**

2. Citations and explanations (Rule 70.7)

- D1: US 2004/0026730 A1 (KOSTYLEV et al), 12 February 2004
- D2: EP 1 202 285 A2 (MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD.), 2 May 2002
- D3: US 6,507,061 (HUDGENS et al), 14 January 2003
- D4: US 5,363,329 A (TROYAN), 8 November 1994
- D5: US 4,203,123 A (SHANKS), 13 May 1980
- D6: US 4,177,475 A (HOLMBERG), 4 December 1979

The above documents represent the closest prior art, and do not anticipate the claimed invention.

CLAIMS

1. A data recording element for a memory cell of a writeable and erasable memory medium comprising:

a laminated structure of at least two multiple-layer structures, each said multiple-layer structure comprising a plurality of individual layers, at least one of the plurality of individual layers in each multiple-layer structure being made of a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse, one of the plurality of individual layers having at least one atomic element which is absent from other one of the plurality of individual layers, and

a final individual layer disposed upon said at least two multiple-layer structures, said final individual layer being formed of the same material of a first individual layer of a first multiple-layer structure of said laminated structure

wherein a crystallization speed of said first individual layer and final individual layer is higher than that of other layers of the multiple-layer structure, and a crystallization temperature of said first individual layer and final individual layer is lower than that of other layers of the multiple-layer structure.

2. The data recording element as recited in claim 1, wherein the plurality of sequentially disposed individual layers are disposed in a same sequence in at least two said multiple-layer structures.

3. The data recording element as recited in claim 1, wherein the plurality of sequentially disposed individual layers are disposed in a different sequence in at least two said multiple-layer structures.

4. The data recording element as recited in claim 1, wherein each individual layer has a thickness in a range of about 0.1 nm to about 10 nm.

5. The data recording element as recited in claim 1, wherein all the individual layers in each said multiple-layer structure have the same thickness.

6. The data recording element as recited in claim 1, wherein any two neighboring individual layers have a ratio of thickness in a range of about 0.1 to about 10.

7. The data recording element as recited in claim 1, wherein the total thickness of the data recording element is in a range of about 5 nm to about 500 nm.

8. The data recording element as recited in claim 7, wherein the total thickness of the individual layers is in a range of about 5 nm to 100 nm.

9. The data recording element as recited in claim 1, wherein at least one of the plurality of individual layers is formed of a material selected from a group consisting of Ge, Te, Sb, Ag, GeTe, SbTe, AgIn, GeSbTe, AgInSbTe, TeAsGe, TeSeS, TeSeSb, InSbTe, TeGeSn, In, Cr, N, Se, Sn, Si, Bi and Ag.

10. The data recording element as recited in claim 1, wherein said at least one of the plurality of individual layers is deposited in a crystalline state.

11. The data recording element as recited in claim 1, wherein a resistance of said at least one individual layer is lower in an crystalline state than that in an amorphous state.

12. (CANCELLED).

13. (CANCELLED).

14. The data recording element as recited in claim 1, wherein the crystallization temperature of said first individual layer and final individual layer is in a range of about 90 °C to 120 °C.

15. The data recording element as recited in claim 1, further comprising an electrode formed adjacent to the data recording element, an edge of the electrode contacting the data recording element for transferring electrical signals between the electrode and the data recording element.

16. The data recording element as recited in claim 1, wherein said laminated structure forms a superlattice-like structure.

17. A data recording element for a memory cell of a writeable and erasable memory medium comprising:

a laminated structure having a first external layer, a second external layer and a plurality of internal layers formed between the first and second external layers, at least one layer of the laminated structure being made of a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse,

wherein said first and second external layers having a relatively high crystallization speed and low crystallization temperature than the internal layers.

18. (CANCELLED).

19. The data recording element as recited in claim 17, wherein the crystallization temperature of said first and second external layers is in a range of about 90 °C to 120 °C.

20. A memory cell for a writeable and erasable memory medium comprising:

a substrate;

first and second contacts formed on said substrate;

a data recording element formed between said first and second contacts, said data recording element comprising a laminated structure of two or more multiple-layer structures and a final individual layer disposed upon said at least two multiple-layer structures; each said multiple-layer structure

comprising a plurality of sequentially disposed individual layers, at least one of said individual layer in each multiple-layer structure being a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse, one of the plurality of individual layers having at least one atomic element which is absent from other one of the plurality of individual layers; said final individual layer being formed of the same material of a first individual layer of a first multiple-layer structure of said laminated structure, wherein a crystallization speed of said first individual layer and final individual layer is higher than that of other layers of the multiple-layer structure, and a crystallization temperature of said first individual layer and final individual layer is lower than that of other layers of the multiple-layer structure;

a high temperature electrode formed adjacent the data recording element; and

an insulating material isolating said memory cell from adjacent memory cells.

21. An electrically writeable and erasable memory medium comprising a plurality of memory cells and an arrangement of conductors such that each memory cell is electrically addressable, each said memory cell comprising

a substrate;

first and second contacts formed on said substrate;

a data recording element formed between said first and second contacts, said data recording element comprising a laminated structure of two or more multiple-layer structures and a final individual layer disposed upon said at least two multiple-layer structures;, each said multiple-layer structure comprising a plurality of sequentially disposed individual layers, at least one of said individual layer in each multiple-layer structure being a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse; one of the plurality of individual layers having at least one atomic element which is absent from other one of the plurality of individual layers; said final individual layer being formed of the same material of a first individual layer of a first multiple-layer structure of said laminated structure, wherein a crystallization speed of said

first individual layer and final individual layer is higher than that of other layers of the multiple-layer structure, and a crystallization temperature of said first individual layer and final individual layer is lower than that of other layers of the multiple-layer structure;

a high temperature electrode formed adjacent the data recording element; and

an insulating material isolating said memory cell from adjacent memory cells.

22. A method of producing a data recording element for a memory cell of electrically writeable and erasable memory medium, the method comprising:

depositing a first multiple-layer structure on a substrate; said multiple-layer structure consisting of at least two individual layers, at least one of said individual layers being a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse;

depositing one or more further multiple-layer structures on said first multiple-layer structure to form a laminated structure, said further multiple-layer structures comprising at least two individual layers, at least one of said individual layers being a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse,

depositing a final individual layer formed of a same material as a first individual layer of said first multiple-layer structure;

wherein one individual layer of said first and further multiple layer structures having at least one atomic element which is absent from another individual layer, and

wherein said first and final individual layers having a relatively high crystallization speed and low crystallization temperature than other layers of the first and further multiple-layer structure..

23. (CANCELLED).

24. (CANCELLED).

25. The data recording element as recited in claim 22, wherein the crystallization temperature of said first and final individual layers is in a range of about 90 °C to 120 °C.

26. A method of producing a memory cell for a writeable and erasable memory medium, comprising:

depositing an insulating material on a substrate;

depositing a first contact on said insulating material;

depositing a high temperature electrode adjacent said first contact;

sequentially depositing two or more multiple-layer structures to form a data recording element, each said multiple-layer structure comprising two or more individual layers, at least one said individual layer in each said multiple-layer structure being formed from a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse; one of the plurality of individual layers having at least one atomic element which is absent from other one of the plurality of individual layers;

depositing a final individual layer formed of a same material as a first individual layer of said first multiple-layer structure; wherein said first and final individual layers having a relatively high crystallization speed and low crystallization temperature than other layers of the first and further multiple-layer structure..

depositing a second contact on said data recording element; and

depositing further insulating material to isolate said memory cell from adjacent memory cells.

27. The method as recited in claim 26, further comprising depositing a final individual layer formed of a same material as a first individual layer of said first multiple-layer structure.

28. A method of writing and erasing information to an electrically writeable and erasable memory medium having a plurality of memory cells and an arrangement

of conductors such that each memory cell is electrically addressable, each memory cell comprising:

a substrate;

first and second contacts formed on said substrate;

a data recording element formed between said first and second contacts, said data recording element having a laminated structure of tow or more multiple-layer structures and a final individual layer disposed upon said at least two multiple-layer structures;, each said multiple-layer structure having a plurality of sequentially disposed individual layers, at least one of said individual layers in each multiple-layer structure being a phase-change material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse, one of the plurality of individual layers having at least one atomic element which is absent from other one of the plurality of individual layers.; said final individual layer being formed of the same material of a first individual layer of a first multiple-layer structure of said laminated structure, wherein a crystallization speed of said first individual layer and final individual layer is higher than that of other layers of the multiple-layer structure, and a crystallization temperature of said first individual layer and final individual layer is lower than that of other layers of the multiple-layer structure; and

a high temperature electrode formed adjacent the data recording element;

the method including:

applying an energy pulse to said data recording element via said high temperature electrode, said energy pulse supplying sufficient energy to change said phase-change material between a crystalline phase and an amorphous phase.

29. The method as recited in claim 28, wherein said energy pulse is a single pulse.

30. The method as recited in claim 28, wherein said energy pulse is a chain of multi-pulses.

31. The method as recited in claim 28, wherein said energy pulse has a duration of less than about 50 ns for data writing.

32. The method as recited in claim 30, wherein said energy pulse has a duration of not more than 7 ns for data writing.

33. The method as recited in claim 28, wherein said energy pulse has a duration of less than about 50 ns for data erasing.

34. The method as recited in claim 32, wherein said energy pulse has a duration of not more than about 10 ns for data erasing.